Control and Stability Analysis for the Vdd-hopping Mechanism

Carolina Albea, Carlos Canudas de Wit and Francisco Gordillo

***Abstract*— In low-power electronics, achieving a high energy efficiency has great relevance. Nowadays, Global Asynchronous Local Synchronous Systems enables to use a Local Dynamic Voltage Scaling architecture. This technique allows to reach a high energy efficiency. Moreover, Local Dynamic Voltage Scaling can be implemented using different approaches. One of them is the Vdd-Hopping technique. In this paper, we propose an innovative control approach which aims for minimizing the energy dissipated during the Vdd-Hopping transients. In addition, our control also includes the ability to limit the current peaks during such transients. Stability of the closed-loop system is analyzed.**

A discrete version of this controller is obtained, which coincides with ENergy-AwaRe Control (ENARC) that is patent pending. And a comparison of this last one with another published is done.

I. Introduction.

The development of low-power electronic needs gigantic number of chips and at the same time every chip should be implemented at the lower power level.

In a chip, several levels of supply voltages are required for reducing power consumption, therefore an integrated DC-DC converter is an important component. These converters have to generate voltages in the typical rage of $0.8V - 2.5V$ from a source of $3.3V$.

The most commonly used topologies in DC-DC converters in low power electronics are: continuous buck converters [1], [2], [3], boost converters [4] and buck-boost converters or charge pump [5], among others. Nevertheless, discrete converters can achieve a larger energy-efficiency, as the Power Supply Selector (PSS) presented in [6], which deal with Local Dynamic Voltage Scaling (LDVS) [7], [8] adapted to Globally Asynchronous and Locally Synchronous Systems (GALS) [9]. This mode of operation provides additional flexibility which allows to use energy-aware converter structures such as Dynamic Voltage Scaling (DVS) architectures.

In this case, LDVS is based on Vdd-hopping technique that fulfills LDVS by dynamically changing the supply voltage V_{dd}. The operation principle is to use two voltage levels instead of a continuously adjustable voltage. Vdd-hopping system is made up of a discrete DC-DC converter called Power Supply Selector with the two voltage levels refereed before.

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The main control problem in low-energy DC-DC converters is to achieve a high energy-efficiency, a low cost and a minimal area occupancy in the silicon-wafer. In addition, DC-DC converters must be able to adapt to various loading conditions and achieve high efficiency over a wide load-current range, which is critical for extended battery life. Moreover, it is also important to keep the rate of change of the device voltage provides a correct and reliable operation during the switch transition.

In this paper, a controller is proposed to handle the two-voltage level Vdd-hopping structure. Nevertheless, an important current peak is obtained. This controller was modified in order to achieve a high-performance from a point of view of current peaks. Current peaks are managed by means of introducing a maximal current peak constraint, that is, introducing an on-line saturation mechanism.

Stability analysis of the closed-loop system is based on LaSalle's invariance principle, both without and with saturation mechanism. The system with the on-line saturation mechanism works as a switched system. In this case, it is proved that the system converges to the voltage reference.

The controller is discretized for physical implementation, reaching the same structure that the patent pending control with the name ENergy-AwaRe Controller (ENARC) [10]. Moreover, it is compared with the discrete one proposed by [6]. Getting a considerable improvement with respect to the energy efficiency as well as providing a safe operation condition, thus, it provides an advance in the energy-aware nanotechnology field.

The rest of this work is organized as follows: in Section II the circuit model of the Vdd-hopping is presented just as its properties and the error equation for achieving the desired voltage levels. This model is used in order to design a robust controller in Section III. Stability analysis is shown in Section IV. A discretization and comparison is made in Section V. The work closes with a section of conclusions.

Notation. Let us denote:

$$\text{sat}_m^M(x) = \begin{cases} M & if \quad x > M \\ x & if \quad m \leq x \leq M \\ m & if \quad x < m \end{cases}$$

round(x) is the nearest integer to x. Finally, ζ^+ and ζ^- respectively denote $\zeta(k+1)$ and $\zeta(k)$, that is, the value of ζ in two consecutive sampling time, furthermore $\Delta\zeta \triangleq \zeta^+ - \zeta^-$.

II. Model of Vdd-hopping mechanism.

The aim of DC-DC converters in portable electronic systems is to obtain a high efficiency, low cost, reduced size and low noise, since the battery capacity is limited in any portable electronic device. These converters can further enhance battery run-time.

A. Mathematical model.

There is a novel discrete DC-DC converter presented in [6] called Power Supply Selector (PSS) which principal advantages are: it has a minimal area occupancy in the silicon-wafer, negligible dissipated energy, low cost and it does not need passive components. It uses Vdd-hopping technique for getting a LDVS architecture for a globally asynchronous and locally synchronous system.

Vdd-hopping is basically made up of a PSS and two external supply voltages which provides a high voltage level, V_{high}, and a low voltage level, V_{low}. For simplicity, only one voltage supply is considered, V_{high}, accomplishing the two voltage levels with this only voltage supply. With this assumption about the supply voltage, at least one transistor must be always switched on. v_c is the output voltage of the system.

The load model for this kind of low-power system usually is an impedance which depends on the chip frequency, and also on the core voltage, v_c. We assume that in the Vdd-hopping system the frequency depends on the v_c, thus, we consider that the load depends only on the v_c. The load model can also be completed with a leakage current source due to the aggregated effect of the PMOS leaks transistors.

B. Mathematical model for control design.

Figure 1 shows an electrical representation of the Vdd-hopping with the voltage supply, V_{high}, together with the load described before.

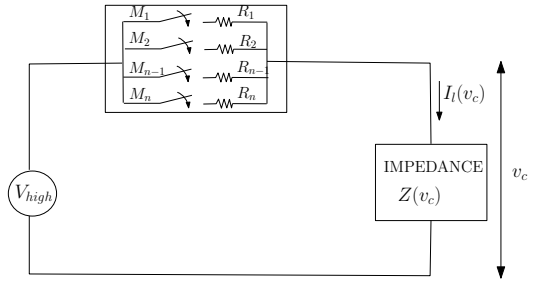

Fig. 1. Vdd-hopping, voltage supply and load

Assumption 1: The PMOS transistors are modeled as ideal resistors when they are switched-on. They are considered to have the same electrical characteristics.

Let us take $V_h = V_{high}$, the voltage loop equation yields the relation:

$$I_l(v_c) = \frac{V_h - v_c}{R(u_k)} \tag{1}$$

where $R(u_k) \triangleq \frac{R_0}{u_k}$ being u_k the number of transistors switched on, therefore, $u_k \in \mathcal{U} = \{1, 2, ..N\}$ and it will be the control law. Note, that with $u_k = 1$ and $u_k = N$ are achieved the desired low and high voltage values, respectively. On the other hand, R_0 is the transistor resistance characteristic, that in this case, is the same for all transistors $R_0 = R_1 = R_2 = \ldots = R_N$.

I_l, that is the current through the load, depends only on the v_c, as was seen before, therefore it will vary during the hopping transitions. Note, that the system is continuous less the controller that is discrete.

Combining the specific form of the load impedance with (1), the voltage dynamic expression can be compactly expressed as:

$$\dot{v}_c = -\beta(v_c)v_c + (V_h - v_c)bu_k - \delta \tag{2}$$

where:

- $\beta(v_c) > 0$ depends on the load.
- b and δ depend on the parameters of the system and both are positives.

Note that (2) is a nonlinear system

$$\dot{v}_c = -f(v_c) + g(v_c)u_k - \delta \tag{3}$$

Property 1: System (3) has the following properties

i) $f : D \to \mathbb{R}^+$ and $g : D \to \mathbb{R}^+$ are globally Lipschitz from a domain $D \subset \mathbb{R}^+$ into $\mathbb{R}^+$
ii) f and g are positive-semidefinite
iii) the state v_c is strictly positive
iv) $\delta \in \mathbb{R}^+$ can be seen as a constant perturbation

Defining $e \triangleq v_r - v_c$, where v_r is the reference voltage signal, let us rewrite System (2)

$$\begin{aligned} \dot{e} &= -(bu_k + \beta(v_c))e \\ &\quad +(bu_k + \beta(v_c))v_r - bV_h u_k + \delta + \dot{v}_r \end{aligned} \tag{4}$$

which is the associated error equation.

In [11] is proved that the error system is open-loop stable.

III. Control law.

As was seen before, System (2) is a stable first order nonlinear system. Nevertheless, in low-power system there is certain requirements like minimal dissipated energy, minimal current peaks through the set of PMOS, minimal transition time, etc, which can be achieved with a suitable control law.

A. Robust control design without current peak constraint.

This controller is designed to cope with possible steady-state errors. It is computed assuming that more than one transistor is switched at once and, dealing with a stabilization point problem. Therefore, the reference will be constant. This controller is not based on the explicit knowledge of the system, being robust.

The proposed control law is:

$$u_k = \text{sat}_1^N \{\text{round}(K_1 e + K_2 \sigma)\} \tag{5}$$

Note, that σ corresponds to $\int_t^{t+T} e$, which augments the system. They are chosen with the follow tunning mechanism:

$$K_1 = \frac{2\xi\omega_n - (u_{k_l} b + \beta_l)}{b(V_{high} - V_{low})} \quad (6)$$

$$K_2 = \frac{\omega_n^2}{b(V_{high} - V_{low})} \quad (7)$$

being $\beta_l = \min(\beta)$. Note that $K_2 > 0$.

Lemma 1: If ξ is chosen such that

$$\xi \in \left[\frac{u_{k_l} b + \beta_l}{2\omega_n}, \frac{u_{k_l} b + \beta_l}{2\omega_n} + \frac{\omega_n^2 b(V_h - V_{low})}{b^2 \bar{u}_k^M (V_h - V_{low})_k + 2\omega_n^2} \right]$$

then $K_1 > 0$ and $K_1(b\bar{u}_k^M + 2K_2) - K_2 < 0$. Being $\bar{u}_k^M$ the maximal equilibrium value of u_k. Note, that $\frac{\omega_n^2 b(V_h - V_{low})}{b^2 \bar{u}_k^M (V_h - V_{low})_k + 2\omega_n^2} > 0$.

A simulation using Matlab is done for displaying the stability properties of this control law.

The number of transistors used is $N = 24$. Note that there is always, at least, one active transistor. The voltage supply is $V_h = 1.2V$. v_r follows a linear time evolution between $V_{low} = 0.8V$ and $V_h = 1.2 - \Delta$.

Remark 1: The maximal voltage achieved, v_c, must be $V_{max} = V_h - \Delta$ where $\Delta \in \mathbb{R}$ being small. It depends on the voltage supply, the PMOS transistors characteristic and the load.

The PMOS transistors have a value $R_0 = 31,4\Omega$, the capacitance is $C = 9nF$, the threshold voltage is $V_{th} = 0.4V$, and clock frequency system is $w_n = 500MHz$. Δ is $0.087V$. $\xi \in [0.04, 0.08]$, and it is taken $\xi = 0.05$.

Figure 2 shows the simulation of this control strategy. This controller does not require model information, thus it is easy for physical implementation, nevertheless it provides an important current peak, which are not desired since it increases the energy dissipated as can damage the physical system.

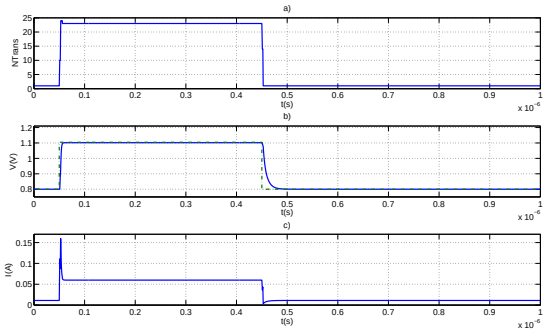

Fig. 2. Control without current peak constraints. a) Evolution of the number of active PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current I_l.

B. Control redesign with current constraint.

In order to avoid current peaks, let us introduce a system with pre-specified constraints. This constraint can be the maximal admissible current peak for the system, $|\Delta I_l|$. This constraint can be introduced in the system defining:

$$I_l^+ = \frac{V_h - v_c^+}{R_0} u_k^+$$

$$I_l^- = \frac{V_h - v_c^-}{R_0} u_k^-$$

Let us regard, that v_c is continuous, that is, $v_c = v_c^+ = v_c^-$ then

$$\Delta I_l = \frac{V_h - v_c}{R_0}(u_k^+ - u_k^-) = \frac{V_h - v_c}{R_0}\Delta u_k$$

The maximal admissible current peak is:

$$\frac{V_h - v_c}{R_0}\Delta u_k \leq |\Delta I_l|$$

being

$$-\Delta I_l \leq \frac{V_h - v_c}{R_0}\Delta u_k \leq \Delta I_l$$

This constraint can be introduced in the system by saturating Δu_k. The maximal and minimal u_k is in every period-time:

$$\Delta u_k^M = \frac{R_0}{V_h - v_c}\Delta I_l \triangleq \alpha_k^M \quad (8)$$

$$\Delta u_k^m = -\frac{R_0}{V_h - v_c}\Delta I_l \triangleq \alpha_k^m \quad (9)$$

being $\alpha_k^M > 0$ and $\alpha_k^m < 0$. Thus, the controller is

$$u_k = \text{sat}_1^N \left\{ \text{round}(\text{sat}_{\bar{\alpha}_k^m}^{\bar{\alpha}_k^M}(K_1 e + K_2 \sigma)) \right\} \quad (10)$$

where the current peak constraints are employed according to next expressions:

$$\bar{\alpha}_k^M = u_{k-1} + \alpha_k^M \quad (11)$$

$$\bar{\alpha}_k^m = u_{k-1} + \alpha_k^m \quad (12)$$

In order to simulate the closed-loop system, we take the maximal admissible current peak for switching, at least, one transistor. For that, $\Delta I_l > \frac{V_h - V_{low}}{R_0} 0.5$. Note, as u_k is an integer, then the minimal Δu necessary for switching is 0.5.

Figure 3 shows a simulation of this controller. Note, how the current peaks have been reduced considerably with respect to the previous controller (Fig. 2).

IV. Stability analysis of the robust controller.

In this section, let us study the stability of System (2) in closed-loop with the robust controller developed in the previous section. Firstly, we are going to analyze the stability of the closed-loop system without on-line current limits saturation, and following, with on-line current limits saturation.

Let us assume that β changes slowly $\dot{\beta} \approx 0$, considering that it is constant.

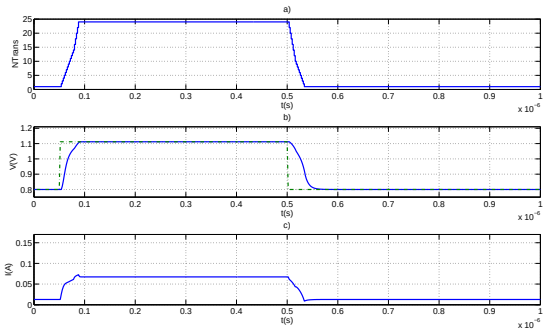

Fig. 3. ENARC. a) Evolution of the number of switched-on PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current

A. Stability of the closed-loop without current peak constraints.

In this point, we are going to deal with stabilization point problem for System (2) with controller (5).

Theorem 1: System (2) with controller (5) is locally asymptotically stable for all initial condition $e(0)$, if K_1 and K_2 are positives.

Proof: The equilibriums of System (2) are

$$0 = -(v_r - V_h)b\bar{u}_k + \beta\bar{v}_c + \delta$$

getting the controller values

$$\bar{u}_k = \frac{\beta\bar{v}_c + \delta}{(V_h - v_r)b} = K_2\bar{\sigma} \tag{13}$$

$\bar{v}_c$ and $\bar{\sigma}$ are the equilibrium value of v_c and σ, respectively. Note that $\bar{u}_k$ will be 1 or N, as has been said in Section before.

Let us take $w_k = u_k - \bar{u}_k$, System (2) reaches the form:

$$\begin{aligned}\dot{e} &= -f(\bar{u}_k + w_k)e + (v_r - V_h)bw_k + \\ &\quad (v_r - V_h)b\bar{u}_k + K_2v_c + \delta \end{aligned} \tag{14}$$

Being $f(\bar{u}_k + w_k)$ positive.

Using (13) in the third term of the right-hand side of (14), we can achieve

$$\dot{e} = -f(\bar{u}_k + w_k)e + (v_r - V_h)bw_k - K_2e$$

Following the Lyapunov's arguments, let us take the next candidate Lyapunov function

$$\begin{aligned}V &= \frac{e^2}{2b(V_h - v_r)} + \frac{(\sigma - \bar{\sigma})^2}{2}K_2 = \\ &\quad \frac{e^2}{2b(V_h - v_r)} + \frac{(u_k - \bar{u}_k - K_1e)^2}{2K_2}\end{aligned}$$

Note that v_r is the reference and it is constant. Moreover, $(V_h - v_r) > 0$ and b is positive as was established in Section II. The second equality comes from (5) and (13), thus the Lyapunov derivative is

$$\begin{aligned}\dot{V} = &-\frac{f(\bar{u}_k + w_k)e^2}{b(V_h - v_r)} - \frac{K_2e^2}{b(V_h - v_r)} - K_1e^2 + \\ &\frac{1}{K_2}\left[(K_1\dot{e} + K_2e) - (K_1\dot{e} + K_2e)\right]\cdot \\ &\left[sat_1^N\{round(K_1e + K_2\sigma)\} - K_2\bar{\sigma} - K_1e\right]\end{aligned}$$

it is reached adding $\pm K_1e^2$ and considering $\dot{u}_k = K_1\dot{e} + K_2e$. Therefore,

$$\dot{V} = -\left(\frac{f(\bar{u}_k + w_k)}{b(V_h - v_r)} + \frac{K_2}{b(V_h - v_r)} + K_1\right)e^2 \leq 0$$

Note that K_1 and K_2 are positives, as is stated in the theorem.

The stability is established by LaSalle's invariance principle, since the maximum invariant set with $\dot{V} = 0$ is the single point $(e = 0, \sigma = \bar{\sigma})$. ■

B. Stability of the closed-loop System with current peak constraints.

Now, we are going to study the stability of System (2) with the controller (10), for the stabilization point problem.

Theorem 2: System (2) with controller (10) is locally asymptotically stable for all initial conditions $e(0)$, if K_1 and K_2 are positives.

Proof: There is a space region, where the system does not saturate in the current peak saturations being applicable Theorem 1. This is the Region I showed in the Fig. 4. Nevertheless, there exist two other regions corresponding to the case when the system saturates in the upper level (Region II), and when the system saturates in the lower level (Region III), being a switched system.

Remark 2: The equilibriums of System (2), that is when $u_k = \bar{u}_k$, are in Region I. This is easy to see in definitions (11)–(12).

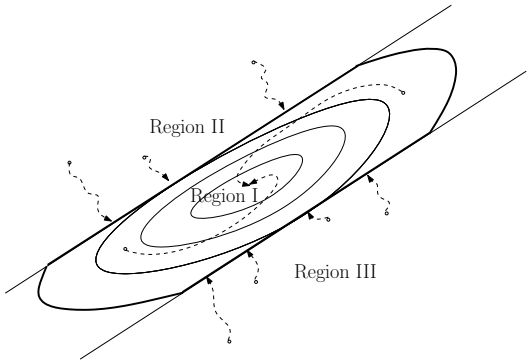

Fig. 4. Saturation system regions

Firstly, let us cope with the Region I. Note that it corresponds to the case studied before, the controller without current peak constraints. Therefore, in this region the system is locally asymptotically stable. Following Remark 2 the equilibriums are in this region.

Next up, the Region II and III are considered. In this case, the saturated system will converge to the Region I in a finite time.

Lemma 2: System (2) with controller (10) saturated in the upper or lower current peak limits for all initial condition $e(0)$ converges to the non-saturation region in a finite time, if $K_1(b\bar{u}_k^M + 2K_2) - K_2 < 0$.

Proof: We start studying the Region II, that is, the case when the system saturates in the upper dynamic limit saturation. Let us regard $\dot{u}_k = K_1\dot{e} + K_2 e$ and that $\alpha_k^M(e)$ is the saturation corresponding to $\dot{u}_k$, as is seen from Eq. (11), then this region has the next property:

Property 2: In Region II, System (2) fulfills

- $\dot{u}_k > \alpha_k^M(e) > 0$
- $\ddot{u}_k \leq \varepsilon < 0$ being $\varepsilon = -bR_0K_1\Delta I_{max} = cte$
- $e > 0$

being $\alpha_k^M(e)$ given by (8). $v_c = v_r - e$, as was seen above. ε comes from $h(e)$ defined below plus Eq. (8).

Remark 3: u_k is monotonous decreasing, with derivative bounded away from zero, as shown the previous property, and hence it will reach $\bar{u}_k$ (Eq. 13) in finite time.

Let us take as Lyapunov function

$$W = \dot{u}_k - \alpha_k^M(e) = K_1\dot{e} + K_2 e - \alpha_k^M(e) > 0$$

derivating (8)

$$\dot{W} = K_1\ddot{e} + K_2\dot{e} + \frac{\alpha_k^M(e)}{(V_h - v_r + e)}\dot{e}$$

substituting the second derivative error

$$\begin{aligned}\dot{W} &= -b(V_h - v_c)K_1\dot{u}_k + \\ &\left(-K_1(bu_k + 2K_2) + K_2 + \frac{\alpha_k^M(e)}{V_h - v_r + e}\right)\dot{e}\end{aligned}$$

Note that $(V_h - v_c) > 0$ and $\dot{u}_k > 0$ in this region, the first term on the right-hand side is negative for all instant time.

Rewriting

$$\begin{aligned}\dot{W} &= -h(e) + \left(-K_1(bu_k + 2K_2) + K_2 + \frac{\alpha_k(e)}{V_h - v_r + e}\right)\dot{e} \\ &< -h(e) + \left(K_1(bu_k + 2K_2) - K_2 - \frac{\alpha_k(e)}{V_h - v_r + e}\right)\frac{K_2 e}{K_1} \\ &< -h(e) + \left(K_1(b\bar{u}_k^M + 2K_2) - K_2 - \frac{\alpha_k(e)}{V_h - v_r + e}\right)\frac{K_2 e}{K_1}\end{aligned}$$

The first inequality comes from $\dot{u}_k > 0$, which is, $K_1\dot{e} + K_2 e > 0$, thus $-\dot{e} < \frac{K_2 e}{K_1}$. In the second inequality, a maximal value of u_k is taken.

As $K_1(b\bar{u}_k^M + 2K_2) - K_2 < 0$ then

$$\dot{W} < 0$$

The proof for Region III is similar to the one developed before for Region II. ■

By La Salle's invariance principle, we can conclude the statement of the Theorem, since we have found an invariant set Ω, see Fig.4, such that $\dot{V}(e,\sigma) = 0 \quad \forall (e,\sigma) \in \Omega$, containing the desired point. Furthermore, Lemma 1 implies that the domain of attraction is not restricted to the invariant set Ω, but it is also limited by the saturation limits and some appropriate Lyapunov levels. ■

V. Discretization and comparison of the controller with current peak constraints.

The controller (10) is discretized for physical implementation, as follows:

$$\bar{u}_k = sat_1^N\left\{\bar{u}_{k-1} + round(sat_{\alpha_m^k}^{\alpha_k^M}(\bar{K}_1\Delta e_k + \bar{K}_2 e_k))\right\} \quad (15)$$

where $\bar{K}_1 = K_1 - \frac{K_2}{2}$, $\bar{K}_2 = K_2 T$ [12].

This controller has a similar structure that the one patent pending in [10], and the simulation of this controller provides a voltage and current evolutions equal that in Fig. 3.

A. Comparison with an intuitive control.

The original problem raised by the authors of [6] is a tracking problem of the voltage v_c with respect to the time-varying reference voltage signal, v_r. The control implemented by the authors is

$$u_{k+1} = u_k + sign(e) \quad (16)$$

as this controller has been designed from intuition, we call it here 'intuitive control'. With this control law, one only transistor can be switched on or off at every sampling time, what is not taken into account for the previous controller, where is assumed that more than one transistor can be switched on or off at the same time period.

Taking the same simulation values given in Section III and having a slope of v_c of $1.015 \cdot 10^6 V/s$, a simulation of this controller is done, which is showed in Fig. 6. Note that the current through the transistors, as expected, presents important peaks.

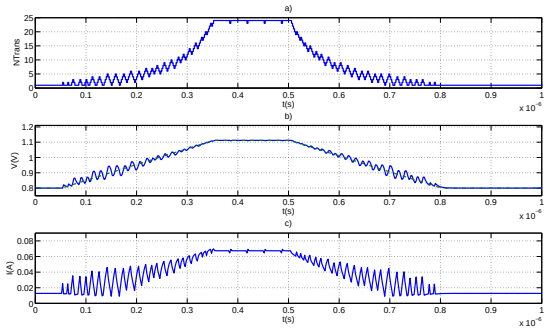

Fig. 6. Intuitive control. a) Evolution of the number of switched-on PMOS, b) evolution of the v_r (dashed) and evolution of v_c (solid). c) evolution of the current I_l.

The dissipated energy during the transient in the set of PMOS depends on the type of control law employed; thus on the switching sequence and the transient time. For

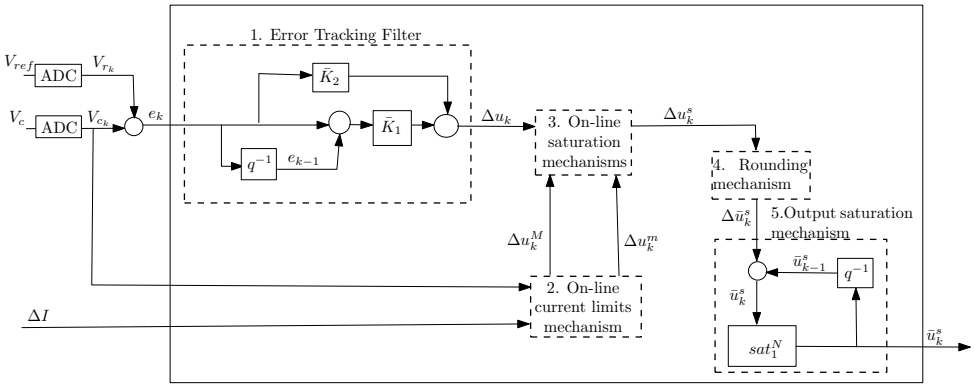

Fig. 5. ENARC structure patented in [10].

instance, a non-smooth behavior of the current transient and a larger transient time may result in a higher energy consumption, as is happened in Fig. 7. In this figure, dissipated energy in the set of PMOS transistors during the rising transient is shown.

Note that the dissipated energy is higher using the intuitive controller (16) than using the discrete-controller (15) providing, besides, a safe operation condition. More precisely, dissipated energy has been reduced from $7.2nJ$ to $0.26nJ$, exactly a 96%.

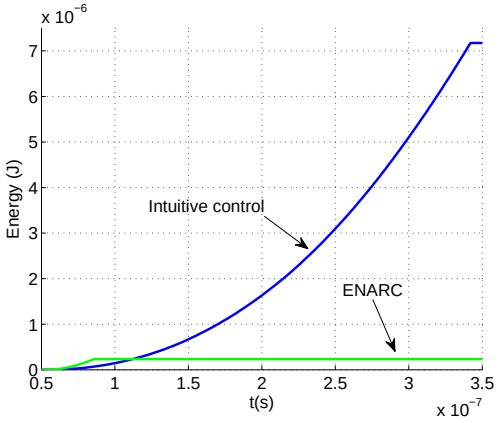

Fig. 7. Energy comparison between the intuitive control, and the ENARC, during rising transient.

VI. Conclusion.

In this work a controller has been designed for the Vdd-hopping system with the aim of reducing the dissipated energy, minimizing the current peaks in the set of PMOS transistors and considering a stabilization-point problem. This last point comes from the possibility of allowing such controller to switch more than one transistor at the same sampling time.

The stability of the Vdd-Hopping system with the proposed controller is analyzed. This analysis follows LaSalle's invariance principle for a domain bounded by Lyapunov level plus saturation lines.

This controller has been discretized, noting that it is similar to the one patented in [10]. Moreover, it has been compared with the discrete intuitive control used in [6], getting a better performance in terms of transient responses and/or dissipated energy.

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